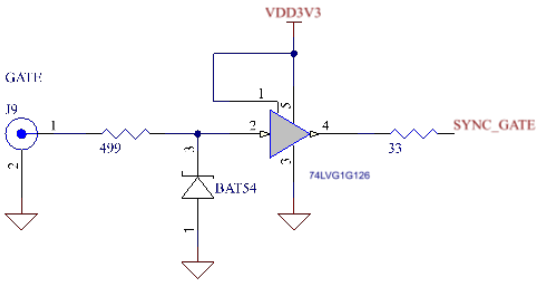
iMS- External Signal Input Levels

The external Gate (J9), Trigger (J10) and Clock (J11) inputs are buffered and optimized for high-speed operation. Noise free input signals are required.
Input circuit shown below.



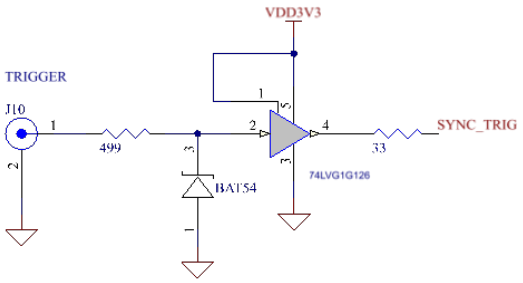
Pre-May 2023:

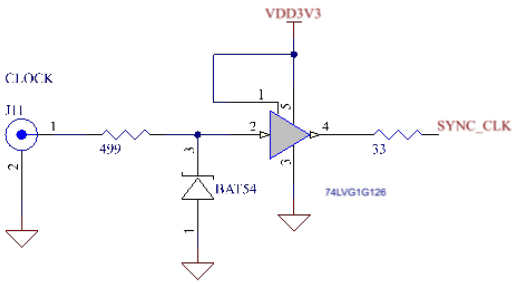
The 74LVC1G126 buffer IC's are 5V tolerant with guaranteed specs for 3V3 supply.

Post-May 2023 update:

To increase noise immunity:

- **Buffer IC's have been replaced with a Schmitt trigger buffer 74LVC1G17**
-
- **Shunt 68pF capacitor is fitted across BAT54 diode.**





Discussion below applies to pre-May 2023 with 74LVG1G126 buffers.

LOW level <0.8V, HIGH level >2.0V.
The input voltage range between 0.8V and 2.0V is indeterminate.

Any ringing or spikes in the range 0.8V – 2.0V may cause a false signal.

In practice, Isomet tests (see page 2) have determined:
Vin > 1.65V with cause a switch from low –> high.
Vin < 1.45V with cause a switch from high –> low.

The SN74L1G126 inputs are high impedance not 50 ohms. The series 499 ohm is current limit protection.
All three signals are over sampled by an internal 75MHz system clock giving a jitter spec of 13nsec.
This provides some immunity, but it is not infallible to all noise on the input signals.

Threshold Testing, Image Mode.
The test Image =12 points; 11 points active RF output + a last point at zero amplitude.

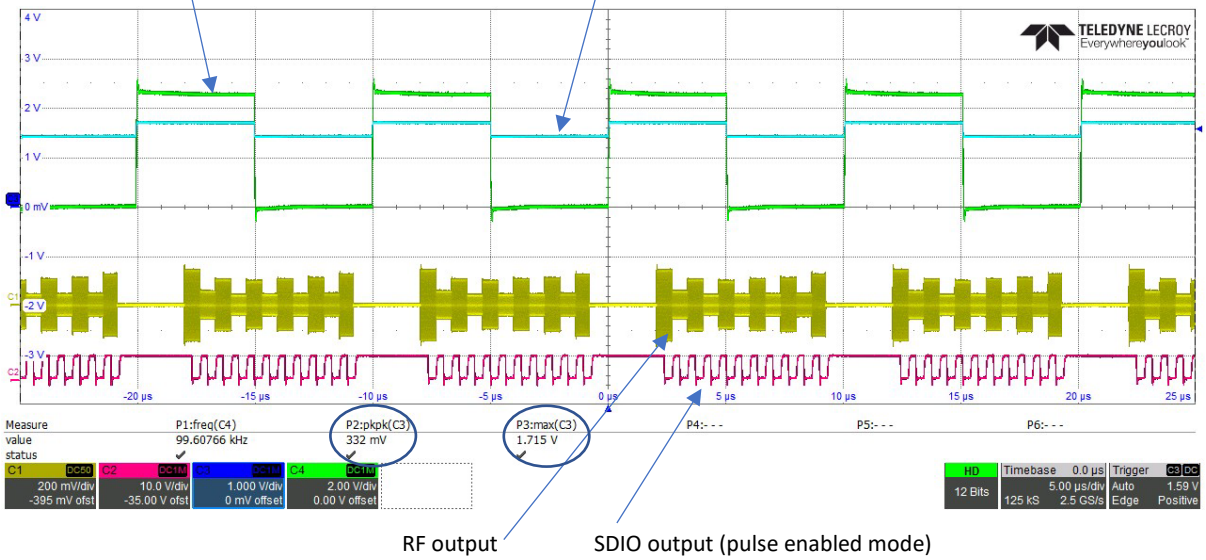
- **Trigger Input**

Internal clock rate = 1.5MHz. External trigger selected.

Maximum trigger rate = 1/(Image points x clock period).
So for a 12 point image, max trigger rate = 125KHz. For clarity a 100KHz trigger rate used below.

An ideal TTL signal (trace C4/green) is shown for comparison only.
(This signal is not connected to the iMS4)

J10, iMS4 Trigger input = trace C3/cyan.
The signal peak-peak voltage level and offset are adjusted to determine switching threshold levels.
Thresholds: OFF = 1.4V <> 1.7V = ON



- **Clock Input**

External trigger 100KHz (a clean TTL input; 0 < Vin < 5V).
The test Image =12 points; 11 points active output + last point zero amplitude.

An ideal TTL signal (trace C4/green) shown for comparison only.
(This signal is not connected to the iMS4)

J11, iMS4 Clock input = trace C3/cyan.
The signal peak-peak voltage level and offset are adjusted to determine switching threshold levels.
Threshold OFF = 1.4V < > 1.7V = ON